AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Currently amended) An integrated circuit comprising [[A]] a capacitor having first and second electrodes, the first electrode being formed of a drain or source region of a MOS transistor formed on the side of a surface of a semiconductor bulk, the second electrode being formed of a conductive region coated with a capacitor dielectric disposed under said drain or source region, in the semiconductor bulk, wherein the insulator coating the lower surface of the coated region exhibits a larger dielectric constant than the insulator coating the rest of the coated conductive region.

2. (Previously Presented) The capacitor of claim 1, wherein the coated conductive region comprises an extension above a portion of which is formed a contact opening towards the second electrode.

3. (Canceled)

4. (Currently amended) An SRAM cell comprising two inverters head-to-tail, each of which comprises two MOS transistors of two conductivity types formed side by side, having their drains connected to each other and having their gates connected to each other, and comprising two capacitors of claim [[3]]1, the respective first electrodes of which are the drains of said transistors and the second electrodes of which are a same coated region connected to the gates of said transistors via a contact opening formed between the two transistors.

5. (Currently amended) A DRAM cell comprising a MOS transistor having its source region connected to a bit line, having its gate connected to a word line, and comprising a capacitor of claim [[3]]1, the first electrode of which is the drain region of said transistor and the second electrode of which is a coated region connected to a supply line.

6. (Canceled)

7. (Previously Presented) A method for manufacturing a capacitor having a first electrode formed of a heavily-doped active region of a semiconductor component, comprising:

a/ forming at the surface of an initial semiconductor substrate a conductive region coated with an insulator;

b/ growing by epitaxy a semiconductor layer to cover the initial substrate and bury the coated region;

c/ forming said heavily-doped active region across the entire thickness of said semiconductor layer, above a portion of the coated conductive region, the heavily-doped active region being insulated from the conductive region.

8. (Previously Presented) The method of claim 7, wherein the heavily-doped active region is one of the drain region and of the source region of a MOS transistor.

9. (Previously Presented) The method of claim 8, wherein, before forming the drain and source regions, an opening is made above another portion of the coated conductive region in said semiconductor layer and in the insulator coating the conductive region to connect the conductive region to a conductive layer used to form the gate of the transistor.

10. (Previously Presented) The method of claim 9, wherein the opening is made at the step of digging the STI insulation trenches of said MOS transistor.

11. (Previously Presented) At least one capacitor formed on an integrated circuit substrate, the at least one capacitor comprising:

a first electrode comprising a drain or source of a MOS transistor;

a first capacitor dielectric region having at least a portion that contacts the first electrode and is buried beneath the first electrode; and

a second electrode buried beneath the first electrode, the second electrode being insulated from the first electrode.

12. (Previously Presented) The at least one capacitor of claim 11, wherein the second electrode is electrically connected to a gate of the MOS transistor.

13. (Previously Presented) The at least one capacitor of claim 11, further comprising:

a third electrode comprising the substrate;

a second capacitor dielectric region buried beneath the second electrode that insulates the second electrode from the third electrode.

14. (Previously Presented) The at least one capacitor of claim 13, wherein a capacitance between the first and second electrodes is different than a capacitance between the second and third electrodes.

15. (Previously Presented) The at least one capacitor of claim 14, wherein the second capacitor dielectric has a higher dielectric constant than the first capacitor dielectric.

16. (Previously Presented) The at least one capacitor of claim 11, wherein the second electrode comprises polysilicon.

17. (Previously Presented) An SRAM cell comprising:

the at least one capacitor of claim 11; and

an inverter comprising:

the MOS transistor comprising a first drain and a first gate, wherein the MOS transistor is a first MOS transistor; and

a second MOS transistor comprising a second drain and a second gate;

wherein the first drain and the second drain are coupled to one another;

wherein the first gate and the second gate are coupled to one another;

wherein the first electrode comprises the first drain and the second drain, wherein the second electrode is buried beneath the first drain and the second drain, and wherein the first and second gates are coupled to the second electrode.

18. (Previously Presented) A DRAM cell comprising:

the at least one capacitor of claim 11, wherein the MOS transistor has a source region that is coupled to a bit line;

wherein the MOS transistor has a gate that is coupled to a word line;

wherein the first electrode is a drain region of the MOS transistor; and

wherein the second electrode is coupled to a supply line.

19. (Previously Presented) A method of forming a buried capacitor comprising first and second electrodes, the method comprising:

(A) forming a conductive region above a substrate, the first electrode comprising the conductive region;

(B) forming an insulating region such that at least a first portion of the insulating region is above the conductive region;

(C) forming a semiconductor region at least partially above the at least a first portion of the insulating region; and

(D) forming a heavily-doped active region in the semiconductor region above the at least a first portion of the insulating region such that the heavily-doped active region contacts the at least a first portion of the insulating region, wherein the second electrode comprises the heavily-doped region, wherein the first and second electrodes are insulated from one another.

20. (Previously Presented) The method of claim 19, wherein forming the conductive region comprises forming a highly-doped polysilicon region.

21. (Previously Presented) The method of claim 19, wherein (B) comprises forming a second portion of the insulating region below the conductive region to insulate the conductive region from the substrate.

22. (Previously Presented) The method of claim 19, wherein (B) comprises oxidizing the conductive region to form the insulating region.

23. (Previously Presented) The method of claim 19, further comprising:

(E) forming a via through the semiconductor region to the at least a first portion of the insulating region;

(F) forming, through the via, an opening in the at least a portion of the insulating region to the conductive region; and

(G) forming, in the via, a conductive region that contacts the conductive region.

24. (Previously Presented) The method of claim 23, wherein (G) is performed concurrently to forming a gate region of a transistor, wherein the highly-doped active region comprises a portion of the transistor.

25. (Previously Presented) The method of claim 23, wherein (G) is performed prior to (D).

26. (Previously Presented) The method of claim 19, wherein the highly-doped active region is formed as a first drain and/or source region of a first MOS transistor.

27. (Previously Presented) The method of claim 26, further comprising:

(H) forming a second MOS transistor comprising a second drain and/or source region;

wherein the first drain and/or source region and the second drain and/or source region are formed such that the via is positioned between the first drain and/or source region and the second drain and/or source region;

wherein both the first drain and/or source region and the second drain and/or source region are formed above respective portions of the conductive region.

28. (Previously Presented) The method of claim 27, wherein (H) comprises forming an inverter of an SRAM memory cell.